



## 3.3V CMOS Static RAM 1 Meg (64K x 16-Bit)

IDT71V016SA/HSA

### Features

- ◆ 64K x 16 advanced high-speed CMOS Static RAM
- ◆ Equal access and cycle times
  - Commercial: 10/12/15/20ns
  - Industrial: 12/15/20ns
- ◆ One Chip Select plus one Output Enable pin
- ◆ Bidirectional data inputs and outputs directly LVTTTL-compatible
- ◆ Low power consumption via chip deselect
- ◆ Upper and Lower Byte Enable Pins
- ◆ Single 3.3V power supply
- ◆ Available in 44-pin Plastic SOJ, 44-pin TSOP, and 48-Ball Plastic FBGA packages

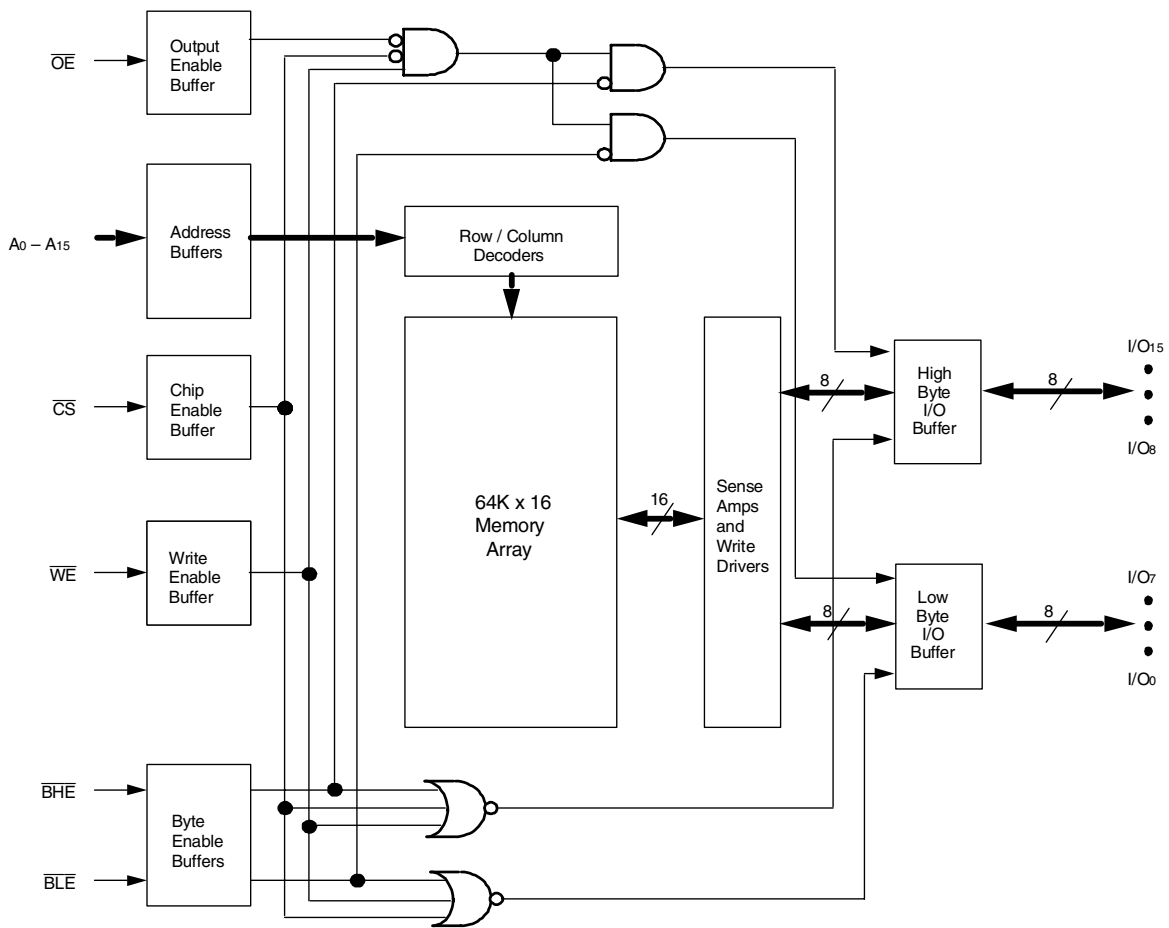
### Description

The IDT71V016 is a 1,048,576-bit high-speed Static RAM organized as 64K x 16. It is fabricated using IDT's high-performance, high-reliability CMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective solution for high-speed memory needs.

The IDT71V016 has an output enable pin which operates as fast as 5ns, with address access times as fast as 10ns. All bidirectional inputs and outputs of the IDT71V016 are LVTTTL-compatible and operation is from a single 3.3V supply. Fully static asynchronous circuitry is used, requiring no clocks or refresh for operation.

The IDT71V016 is packaged in a JEDEC standard 44-pin Plastic SOJ, a 44-pin TSOP Type II, and a 48-ball plastic 7 x 7 mm FBGA.

### Functional Block Diagram



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### Absolute Maximum Ratings<sup>(1)</sup>

Symbol	Rating	Value	Unit
V <sub>DD</sub>	Supply Voltage Relative to V <sub>SS</sub>	-0.5 to +4.6	V
V <sub>IN</sub> , V <sub>OUT</sub>	Terminal Voltage Relative to V <sub>SS</sub>	-0.5 to V <sub>DD</sub> +0.5	V
T <sub>BIAS</sub>	Temperature Under Bias	-55 to +125	°C
T <sub>STG</sub>	Storage Temperature	-55 to +125	°C
P <sub>T</sub>	Power Dissipation	1.25	W
I <sub>OUT</sub>	DC Output Current	50	mA

**NOTE:**

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- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

### Capacitance

(T<sub>A</sub> = +25°C, f = 1.0MHz, SOJ package)

Symbol	Parameter <sup>(1)</sup>	Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 3dV	6	pF
C <sub>I/O</sub>	I/O Capacitance	V <sub>OUT</sub> = 3dV	7	pF

**NOTE:**

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- This parameter is guaranteed by device characterization, but not production tested.

### Recommended Operating Temperature and Supply Voltage

Grade	Temperature	V <sub>SS</sub>	V <sub>DD</sub>
Commercial	0°C to +70°C	0V	See Below
Industrial	-40°C to +85°C	0V	See Below

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### Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V <sub>DD</sub> <sup>(1)</sup>	Supply Voltage	3.15	3.3	3.6	V
V <sub>DD</sub> <sup>(2)</sup>	Supply Voltage	3.0	3.3	3.6	V
V <sub>SS</sub>	Ground	0	0	0	V
V <sub>IH</sub>	Input High Voltage	2.0	—	V <sub>DD</sub> +0.3 <sup>(3)</sup>	V
V <sub>IL</sub>	Input Low Voltage	-0.3 <sup>(4)</sup>	—	0.8	V

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**NOTES:**

- For 71V016SA10 only.
- For all speed grades except 71V016SA10.
- V<sub>IH</sub> (max.) = V<sub>DD</sub>+2V for pulse width less than 5ns, once per cycle.
- V<sub>IL</sub> (min.) = -2V for pulse width less than 5ns, once per cycle.

### DC Electrical Characteristics

(V<sub>DD</sub> = Min. to Max., Commercial and Industrial Temperature Ranges)

Symbol	Parameter	Test Condition	IDT71V016SA		Unit
			Min.	Max.	
I <sub>L</sub>	Input Leakage Current	V <sub>DD</sub> = Max., V <sub>IN</sub> = V <sub>SS</sub> to V <sub>DD</sub>	—	5	μA
I <sub>O</sub>	Output Leakage Current	V <sub>DD</sub> = Max., $\overline{CS}$ = V <sub>IH</sub> , V <sub>OUT</sub> = V <sub>SS</sub> to V <sub>DD</sub>	—	5	μA
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 8mA, V <sub>DD</sub> = Min.	—	0.4	V
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -4mA, V <sub>DD</sub> = Min.	2.4	—	V

### DC Electrical Characteristics<sup>(1,2)</sup>

(V<sub>DD</sub> = Min. to Max., V<sub>LC</sub> = 0.2V, V<sub>HC</sub> = V<sub>DD</sub> - 0.2V)

Symbol	Parameter	71V016SA10				71V016SA12		71V016SA15		71V016SA20		Unit
		Com'l Only		Com'l	Ind	Com'l	Ind	Com'l	Ind			
I <sub>CC</sub>	Dynamic Operating Current CS ≤ V <sub>LC</sub> , Outputs Open, V <sub>DD</sub> = Max., f = f <sub>MAX</sub> <sup>(3)</sup>	Max.	160	150	160	130	130	120	120	mA		
		Typ. <sup>(4)</sup> (5)	65	60	--	55	--	50	--			
I <sub>SB</sub>	Dynamic Standby Power Supply Current CS ≥ V <sub>HC</sub> , Outputs Open, V <sub>DD</sub> = Max., f = f <sub>MAX</sub> <sup>(3)</sup>	45		40	45	35	35	30	30	mA		
I <sub>SB1</sub>	Full Standby Power Supply Current (static) CS ≥ V <sub>HC</sub> , Outputs Open, V <sub>DD</sub> = Max., f = 0 <sup>(3)</sup>	10		10	10	10	10	10	10	mA		

**NOTES:**

- All values are maximum guaranteed values.
- All inputs switch between 0.2V (Low) and V<sub>DD</sub> - 0.2V (High).
- f<sub>MAX</sub> = 1/trc (all address inputs are cycling at f<sub>MAX</sub>); f = 0 means no address input lines are changing.
- Typical values are based on characterization data for H step only measured at 3.3V, 25°C and with equal read and write cycles.

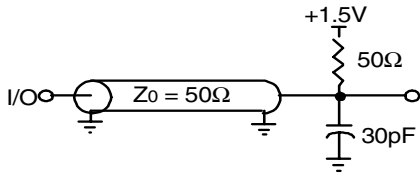
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## AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	1.5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figure 1, 2 and 3

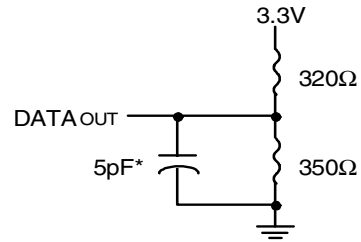
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## AC Test Loads



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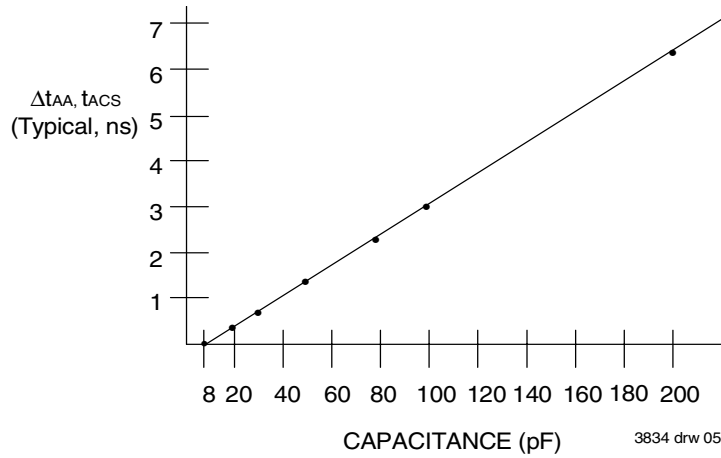
Figure 1. AC Test Load



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\*Including jig and scope capacitance.

Figure 2. AC Test Load  
(for tCLZ, tOLZ, tCHZ, tOHZ, tOW, and tWHZ)



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Figure 3. Output Capacitive Derating

### AC Electrical Characteristics (V<sub>DD</sub> = Min. to Max., Commercial and Industrial Temperature Ranges)

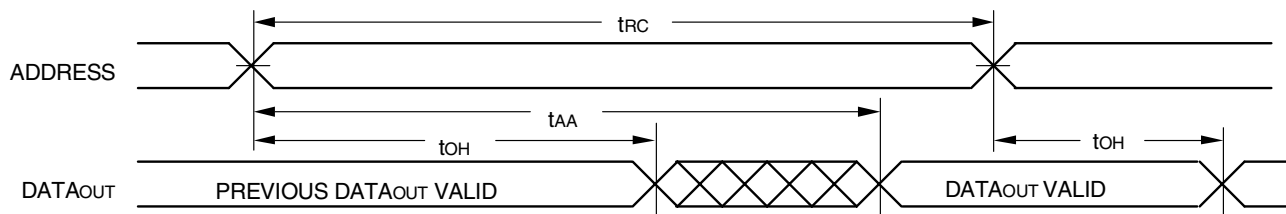
Symbol	Parameter	71V016SA10 <sup>(2)</sup>		71V016SA12		71V016SA15		71V016SA20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
<b>READ CYCLE</b>										
t <sub>RC</sub>	Read Cycle Time	10	—	12	—	15	—	20	—	ns
t <sub>AA</sub>	Address Access Time	—	10	—	12	—	15	—	20	ns
t <sub>ACS</sub>	Chip Select Access Time	—	10	—	12	—	15	—	20	ns
t <sub>CLZ</sub> <sup>(1)</sup>	Chip Select Low to Output in Low-Z	4	—	4	—	5	—	5	—	ns
t <sub>CHZ</sub> <sup>(1)</sup>	Chip Select High to Output in High-Z	—	5	—	6	—	6	—	8	ns
t <sub>OE</sub>	Output Enable Low to Output Valid	—	5	—	6	—	7	—	8	ns
t <sub>OLZ</sub> <sup>(1)</sup>	Output Enable Low to Output in Low-Z	0	—	0	—	0	—	0	—	ns
t <sub>OHZ</sub> <sup>(1)</sup>	Output Enable High to Output in High-Z	—	5	—	6	—	6	—	8	ns
t <sub>OH</sub>	Output Hold from Address Change	4	—	4	—	4	—	4	—	ns
t <sub>BE</sub>	Byte Enable Low to Output Valid	—	5	—	6	—	7	—	8	ns
t <sub>BLZ</sub> <sup>(1)</sup>	Byte Enable Low to Output in Low-Z	0	—	0	—	0	—	0	—	ns
t <sub>BHZ</sub> <sup>(1)</sup>	Byte Enable High to Output in High-Z	—	5	—	6	—	6	—	8	ns
<b>WRITE CYCLE</b>										
t <sub>WC</sub>	Write Cycle Time	10	—	12	—	15	—	20	—	ns
t <sub>AW</sub>	Address Valid to End of Write	7	—	8	—	10	—	12	—	ns
t <sub>CW</sub>	Chip Select Low to End of Write	7	—	8	—	10	—	12	—	ns
t <sub>BW</sub>	Byte Enable Low to End of Write	7	—	8	—	10	—	12	—	ns
t <sub>AS</sub>	Address Set-up Time	0	—	0	—	0	—	0	—	ns
t <sub>WR</sub>	Address Hold from End of Write	0	—	0	—	0	—	0	—	ns
t <sub>WP</sub>	Write Pulse Width	7	—	8	—	10	—	12	—	ns
t <sub>DW</sub>	Data Valid to End of Write	5	—	6	—	7	—	9	—	ns
t <sub>DH</sub>	Data Hold Time	0	—	0	—	0	—	0	—	ns
t <sub>OW</sub> <sup>(1)</sup>	Write Enable High to Output in Low-Z	3	—	3	—	3	—	3	—	ns
t <sub>WHZ</sub> <sup>(1)</sup>	Write Enable Low to Output in High-Z	—	5	—	6	—	6	—	8	ns

**NOTES:**

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1. This parameter is guaranteed with the AC Load (Figure 2) by device characterization, but is not production tested.
2. 0° C to +70° C temperature range only.

### Timing Waveform of Read Cycle No. 1<sup>(1,2,3)</sup>

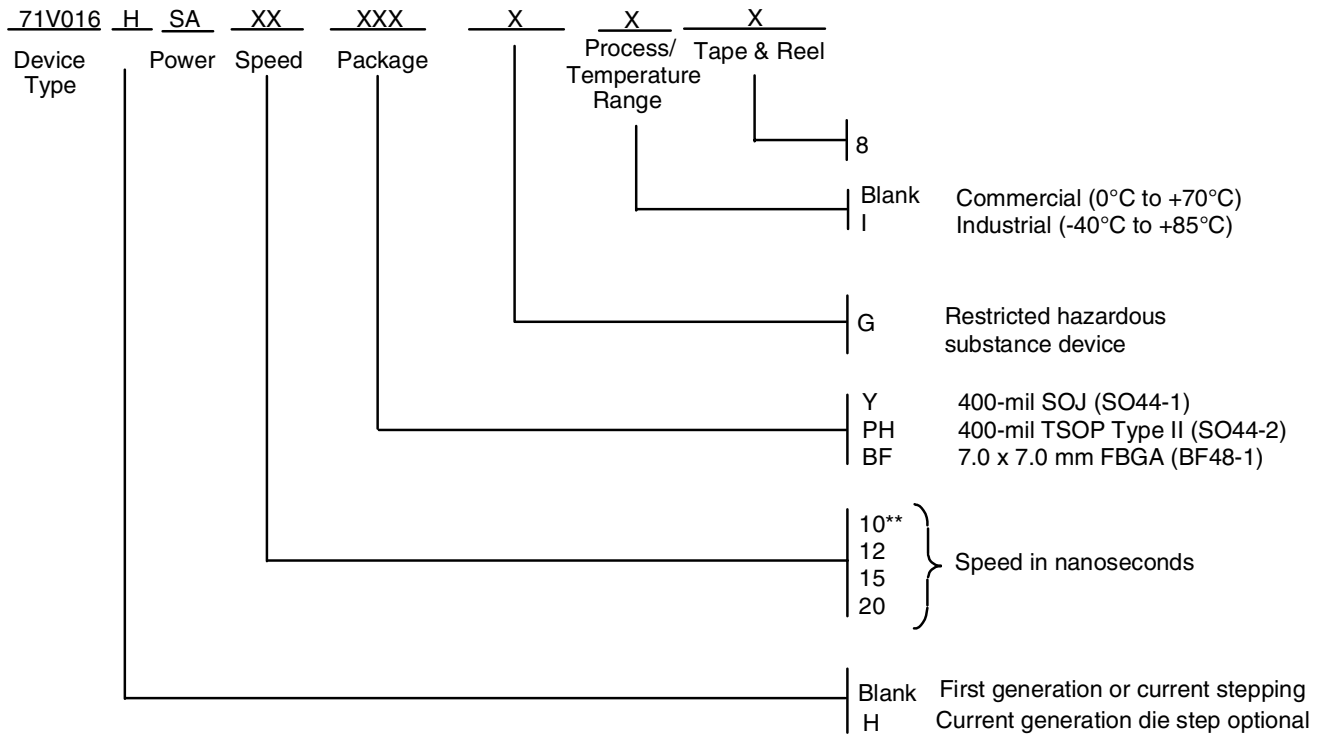


**NOTES:**

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1.  $\overline{WE}$  is HIGH for Read Cycle.
2. Device is continuously selected,  $\overline{CS}$  is LOW.
3.  $\overline{OE}$ ,  $\overline{BHE}$ , and  $\overline{BLE}$  are LOW.

## Ordering Information



\*\* Commercial temperature range only.  
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